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L3	446	716/14	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:05
L4	5	(716/13).ccls. and (ASIC same route) and (buffer or repeater)	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:11
L5	6	(716/12).ccls. and (ASIC same route) and (buffer or repeater)	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:07
L6	2	(716/14).ccls. and (ASIC same route) and (buffer or repeater)	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:07
L7	63	("716"/\$).ccls. and (ASIC same route) and (buffer or repeater)	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:07
L8	264	(ASIC same route) and (buffer or repeater)	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:07
L9	9	(ASIC same route) and (buffer or repeater) and (transmission adj line)	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:10
L10	1	(ASIC same route) same (buffer or repeater) same (transmission adj line)	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:13
L11	3	(716/13).ccls. and ((ASIC same route) same (buffer or repeater))	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:12
L12	2	(716/12).ccls. and ((ASIC same route) same (buffer or repeater))	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:13
L13	0	(716/14).ccls. and ((ASIC same route) same (buffer or repeater))	US-PGPUB; USPAT	OR	OFF	2005/05/25 12:13
L14	0	(716/14).ccls. and ((ASIC same route) same (buffer or repeater))	EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/25 12:13
L15	0	(ASIC same route) same (buffer or repeater) same (transmission adj line)	EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/25 12:13

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1. **An adaptive CMOS transmission line driver**
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2. **Optimum repeater insertion based on a CMOS delay model for on-chip RLC inter**
Ismail, Y.I.; Friedman, E.G.;
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13-16 Sept. 1998 Page(s):369 - 373
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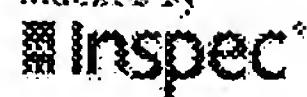
3. **Embedded at-speed test probe**
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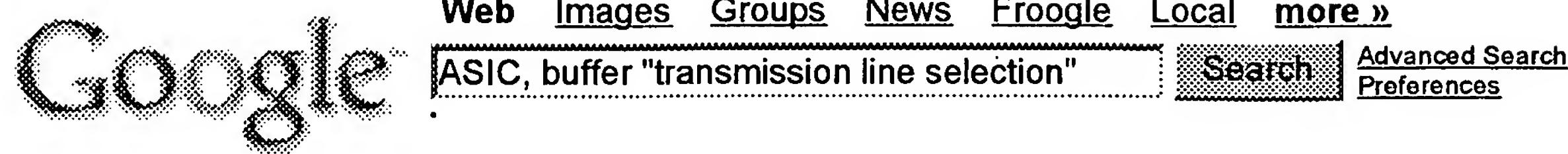
4. **Package clock distribution design optimization for high-speed and low-power VL**
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